High/Low Level Design

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| 2/13/18 | Document created | Matthew Michaels, Reagan Craddock, Milton Griffin, Michael Farden, Matthew Strenk |
| 2/27/18 | Made small revisions, and added trace file and memory description files to document in appendix | Matthew Michaels |
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# Architecture/High Level Design

## Design Goals and Assumptions

* + 1. Goals

One of the main goals of this design is to be able to simulate both cache memory and scratchpad memory within the same application. Another goal of this design is to be able to give the user statistics about the simulation, so that the performance of cache memory and scratchpad memory can be compared. The last goal of this design is that it is multi core meaning that it is able to utilize two system cores at the same time improve performance.

* + 1. Assumptions

The two assumptions of the system are that the user will be given predefined files describing the cache memory and scratchpad memory to be used for the simulation, and that the user will be given a predefined trace file that can be used to simulate the memory. These three files can be seen in the Appendix section of the document.

## System and Component Interaction

The overall system will be comprised of two main pieces, a python script, that will handle user interaction, will integrate the multicore functionality, and that will launch the memory simulator itself, and the memory simulator which is ada based. The python script will start by prompting the user to determine what kind of simulation they would like to run. The user will be given a few options of ways to simulate the memory: hash, heap, mm, stride, or trace and then prompted about any other options if necessary. To go along with each type of simulation, there will be a description of what each type of simulation is so the user has a general idea of how the memory is being tested. After the user has chosen what type of simulation to run, the memory simulator will be launched, and begin simulating both cache memory and scratchpad memory using the same type of simulation. After the simulations have both completed, the application will give the user back results such as, hits and misses, how many cycles it took to complete the simulation, etc. The results will be given back to the user in a command window.

## Rationale and Final Architecture Solution

The system will be based off of an open-source memory simulator written in ada. In order to eliminate the need to interface ada with C, and to give the user the option to customize benchmark types, the multicore handling will implemented in a Python script using the *multiprocessing* package. Because data files will be predefined, this also allows the user to not have to worry about too many inputs for ease of use. The user will be given a prompt when the script is run to input the benchmark type within the console, which will then be stored and passed into the *memsim* application using default values for cache and scratchpad memory. This will then automatically run both simulations on dual cores. Since the idea of simulation is generally to test the feasibility of a certain architecture, performance data will be output to the user and stored in a log file.

# Low Level Design

## Logic and Structure

The program is implemented in Ada 2005. There are two main package hierarchies: the Memory package to describe memories and the Benchmark package to describe benchmarks. The Parser package, which uses the Lexer package, is used to build up memories. In addition, the Test package contains unit tests for the various components.

To generate a simulation, memory type attributes and trace specifications create a simulation hierarchy. In other words, the system first deciphers the type of memory (cache or SPM) that is to be simulated, then allocates the amount of memory specified in the memory configuration file. The default memory size will be set to 5 Megabytes for both the cache memory and the scratchpad memory. The function block diagram for the system is shown below in Fig. 1.

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| --- |
|  |
| Fig. 1: Functional Block Diagram |

In *Figure 1* above, the python module runs the cache memory simulation on the first core and runs the SPM simulation on the second core. The python script will ask the user for the type of benchmark they want to run for the cache and SPM simulators. Each of the simulations take a memory text file as an input, the cache and SPM simulations will have different files. The simulators output into a file which the python module will read in a display in the terminal window.

## Performance

Multiple tests can be run using the same memory file. Scratchpad and cache simulations are run concurrently on multiple cores. The simulation will not take longer than one minute for any test. Simulation statistics will be shown in the command window once the simulations have finished. Log files will we overwritten when the next test is run.

## Interface and Usability

* + 1. Interface  
        The application will be a Python script that is launched in a terminal window. When the application is launched it will prompt the user for information about what kind of simulation they would like to run to compare cache memory and scratchpad memory. After the user has given their input, based on what kind of simulation they would like to run, our actual memsim program will be called from the python script with appropriate inputs to run the desired simulation. When the memsim program has finished running it will print the results of the simulation into the command window so that the user can compare the results of the cache memory to the results of the scratchpad memory.The memsim program is executed by the Python script using the following argument format: ./memsim [<options>] <memory> { <benchmark> [<options>] }.
    2. Usability  
        To run a cache simulation, the memory file must contain the following parameters: *memory, latency, associativity, line\_count, and line\_size*. The *memory* parameter defines the type of memory to be simulated (in this case cache). The *latency* parameter is the delay time between the moment a memory controller tells the memory module to access a particular memory column and the moment that the data is in the correct address. The *associativity* parameter sets the associative value of the cache, defaulting to 1. The *line\_count* parameter refers to the number of cache lines and the *line\_size* parameter refers to size of each cache line in bytes.

To run a scratchpad (SPM) simulation, the memory file must contain the following parameters: *memory, size, and latency.* The *memory* parameter defines the type of memory to be simulated (in this case SPM). The *size* parameter dictates the size of the scratchpad in bytes. The *latency* parameter defines the latency of a hit in the scratchpad.

The trace file that can be used to test the memory will contain read, write, idle time commands in sequence. It must be in the following format: R<address>:<size>, W<address>:<size>, I<cycles>. For read and write commands (denoted as R and W respectively), <address> is the address in hexadecimal and <size> is the size of the memory access in hexadecimal. For the idle command (I), <cycles> is the number of nop cycles in hexadecimal. The user will be given a few options of ways to simulate the memory: hash, heap, mm, stride, or trace and then prompted about any other options if necessary.

## Testability and Maintenance

* + 1. Testability

The testing of the system is based on the memory file, which describes the memory, and the type of test that is used for simulation. The memory file contains specific instructional commands that set the memory system to be simulated (SPM or Cache), the RAM latency, and the size of the data to read/write. The trace file that can be used for testing contains specific memory addresses, read/write commands, and logical iterators to execute. The system can be tested using the following test methods:

|  |
| --- |
| 1. *hash*: A benchmark to generate random 4-byte memory accesses. 2. *heap*: A benchmark to perform random insertions and deletions of 4-byte items in a full binary heap. 3. *stride*: A benchmark to perform strided 4-byte memory accesses. 4. *trace*: A benchmark to execute a memory access trace. |

The results of each simulation are returned after completion. After the simulations have both completed, the application will give the user results such as, hits and misses, how many cycles it took to complete the simulation, etc. This allows us see the speed and accuracy of each memory simulation.

* + 1. Maintenance

The purpose of the simulations is to see the efficiency and quality of each memory system. Since this is a closed system, each simulation is executed in a controlled environment. From a maintainability standpoint, this system is difficult to break. It is easy to restore to an operational state since the system only depends on two outside files, the memory file and the trace file. The simulator itself is also an executable that runs directly in the command line, effectively removing the chance for a compilation error.

## Requirements Tracing

* + 1. The following table’s requirement descriptions and numbers come directly from the Project Requirements document.

|  |  |  |
| --- | --- | --- |
| Requirement number | Requirement description | Element of design to meet requirement |
| 3.1.1 | The system will simulate a multi-core cache/scratchpad. | Python script that runs in two cores and simultaneously simulates both cache and scratchpad memory |
| 3.1.2 | The system will simultaneous run a scratchpad simulation and a cache simulation each time it is run | Python script that runs in two cores and simultaneously simulates both cache and scratchpad memory |
| 3.1.3 | The user will chose what kind of simulation they would like to run by entering a 1, 2, 3, or 4 which each correspond to a type of simulation | Built in user interface that allows the user to select what type of test they would like to run |
| 3.1.4 | The system will check to ensure the user enters correct data and it will exit if the entered data is incorrect | User interface will have built in input detection to ensure the given input is acceptable. |
| 3.1.5 | The system will run the same type of simulation on both the cache and scratchpad memory | Python script will take the user input and tell the simulator to run the same design on both memory types |
| 3.1.6 | The user will have five different ways to simulate the memories: hash, mm, strid, and trace | The memory simulator is already built to only run these types of simulations |
| 3.1.7 | The predefined trace file that can be used to simulate the memory will be formatted in the following way: R/W<address>:<size> or I<cycles> | The file will be predefined this way |
| 3.2.1 | The utility will be run via command line by calling the Python script that controls the simulator | This will be the instructions given to the user, and the design will have no real GUI so this is the method that it will operate |
| 3.2.2 | The command line interface will display statistics based on the results of each simulation | The python script will grab the output from the simulator in the log files and parse it and forward it on to the user in the command window |
| 3.3.1 | The utility will simulate a two core system | The Python script will run two simulators simultaneously in their own cores |
| 3.3.2 | Each simulated core will simulate one of the two memory types | The simulators can only simulate only memory type at a time, so in order to test both memory types at the same type, each core will only simulate one type of memory |
| 3.3.3 | After the simulations are completed, the results will be displayed to the command line | The python script will grab the output from the simulator in the log files and parse it and forward it on to the user in the command window |

## References

* Wingbermuehle, Joe. “Memory Simulator and Optimizer.” Memsim, Github Repository, 24 Sept. 2013, github.com/joewing/memsim.
* “CAS latency.” Wikipedia, Wikimedia Foundation, 13 Feb. 2018, en.wikipedia.org/wiki/CAS\_latency.

## Appendix

* 1. Cache Memory Description File

;

; Cache memory configuration.

;

(dup

(stats

(prefetch (stride 0)

(memory

(cache (latency 1) (associativity 1) (line\_count 4) (line\_size 8)

(memory

(ram (latency 100))

)

)

)

)

)

(ram (latency 50))

)

* 1. Scratchpad Memory Description File

;

; Scratchpad memory configuration.

;

(dup

(stats

(prefetch (stride 0)

(memory

(spm (size 32) (latency 1)

(memory

(ram (latency 100))

)

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)

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)

(ram (latency 50))

)

* 1. Trace file

W0:4

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W8:4

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R0:4

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Wc:4

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W4:4

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W0:4

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R8:4

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W10:4

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Rc:4

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W18:4

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